PROCESS FOR FORMING FAST RECOVERY DIODE WITH A SINGLE LARGE AREA P/N JUNCTION

RELATED APPLICATION

[0001] This application is a divisional of U.S. Patent Application Serial No. 10/115,757, filed April 2, 2002, which is based upon and claims priority to U.S. Provisional Application Serial No. 60/280,972, filed April 2, 2001.

FIELD OF THE INVENTION

[0002] This invention relates to semiconductor devices and processing and more specifically relates to a low cost process for the manufacture of a fast recovery diode and to a novel fast recovery diode structure.

BACKGROUND OF THE INVENTION

[0003] Fast recovery diodes are well known. The processes used for the manufacture of such devices frequently employ cellular and/or stripe and/or trench technologies in a silicon die with electron irradiation for lifetime killing. Such devices use a high mask count and are relatively expensive.

[0004] It would be desirable to make a fast recovery diode (FRED) with a reduced mask count and lifetime killing but with equal or better characteristics to those of existing FRED devices.

BRIEF DESCRIPTION OF THE INVENTION

[0005] In accordance with the invention a novel FRED is formed using a simple single large area junction with platinum lifetime killing. A simplified termination structure is employed using a simple field plate termination at low

voltages (200 volts); amorphous silicon on the field plate at intermediate voltage (400 volts); and plural floating guard rings and an equipotential ring in the cutting street in a higher voltage (600 volts) device. Three, four and five masks are used for the 200 volt, 400 volt and 600 volt devices respectively. Excellent characteristics, equivalent to or better than those of existing FREDs with higher mask counts, are obtained.

BRIEF DESCRIPTION OF THE DRAWINGS

[0006] Figure 1 is a cross-section of a portion of a novel FRED die made in accordance with the invention by a 3 mask process for a 200 volt device.

[0007] Figure 2 is a cross-section of a portion of a novel FRED die made in accordance with the invention by a 4 mask process for a 400 volt device.

[0008] Figure 3 is a cross-section of a portion of a novel FRED device made in accordance with the invention by a 5 mask process for a 600 volt device.

DETAILED DESCRIPTION OF THE DRAWINGS

[0009] Figure 1 shows, in cross-section, a portion of a fast recovery diode die 50 and its termination. The diode consists of a simple large area P type diffusion 51 in an N type epitaxial layer 100 atop the die 50. Diffusion 51 is a boron diffusion having a depth of 6μm and a peak concentration of 2E19/cm^3. A field oxide 54 is formed atop the silicon surface and a conductive (aluminum) field plate 52 which is an extension of the anode electrode is also formed. A metal (aluminum) EQR ring 53 completes the termination. An anode contact is connected to the P type diffusion 51 over substantially the full top area of die 50 and a cathode contact (not shown) is connected to its bottom surface. Platinum atoms are diffused into the back surface of the die (wafer) which are driven in from a 10Å thick layer of platinum for

30 minutes at 950°C. Note that the dimensions on Figure 1 (and Figures 2 and 3) are out of scale and are in microns.

[0010] The novel structure of Figure 1 is made by the following novel 3 mask process of the invention for a FRED rated at 200 volts. The starting wafer has an N^+ arsenic doped substrate which has an N^- phosphorus doped epitaxial layer 100. The epitaxial layer thickness is 25μm and has a resistivity of 10 ohm-cm. The process steps used are given in the following Table:

STEP	**NOTE**
Field Ox 54	Oxide grown to 1.4 um thick
MASK 1	
Oxide Etch	BOE Etch;17 minutes
BBr3 Preclean	Time out 2 h before a BBr3 dep
BBr3 Dep	Target sheet resistance 55 ohm/square
BBr3 Deglass	4 min etch in 50:1 H2O:HF, 15 min timeout after BBr3 Dep
BBr 3 Ox preclean	time out 2 h before BBr3 ox
BBr 3 Ox	Target xj = 5 um
POC13 dep	Target sheet resistance 14.5 ohm square
POC13 deglass	Etch time 1 min. time out after POC13 dep 2 hrs.
POC13 OX	Dry oxidation. Oxide thickness 100 A.
MASK 2	(open active area and termination)
Oxide Etch	Etch time 15 min
Preclean	50:1 H2O:HF
Pt. evap	10 Å on wafer back.
Platinum drive in	30 min at 950°C. Quick extraction.

Preclean	50:1 H2O:HF
Al/Si sputter (52)	Al/Si sputtering, 3 um thickness
MASK 3	
Al etch	7 min in aluminum etch solution
Defreckle	1 min in Ashland Defreckle solution
Photoresist Strip	Standard process
Al sinter	30 min, 420 °C, Forming gas atmosphere.
Wafer Tape	Tape on wafer front
Wafer backgrind	14 mil
Wafer detape	Standard process
Backside metal	CrNiAg sputtering.
Test	Probe Test for 200 V FRED.

[0011] Figure 2 shows a cross-section like that of Figure 1, but with a termination modified to make the device a 400 volt device with a 4 mask process. Components similar to those of Figure 1 have similar identifying numerals.

[0012] In order to withstand 400 volts, the device of Figure 2 employs an added diffusion defining termination P ring 60, an added field plate 61 and an amorphous silicon layer 63 on top of the termination surface, including field plates 52 and 61 and EQR ring 53.

[0013] The device of Figure 2 is made by a novel 4 mask process to increase the device rating to 400 volts. The process begins with a wafer like that of Figure 1, except that the epitaxial layer 100 is 47μm thick, and has a resistivity of 15 ohm-cm.

[0014] The process for the devices of Figure 2 starts with steps 1 to 22 above up to ("photorest strip" and before "Al sinter") for the device of Figure 1.

Following step 22, and before Al sinter, a layer 63 of amorphous silicon, 1800Å thick, is deposited atop the wafer surface. A mask 4 step is then carried out to etch the amorphous silicon to open the active area; specifically, a wet etch (DFK) process.

[0015] Figure 3 is a cross-section like that of Figures 1 and 2 with elements added to permit the device to operate at 600 volts. The process used is a 5 mask process. The elements added are P diffusion rings 70 to 73 and N^+ diffusion 74 in the cutting street and surrounding the die edge to act as an N^+ EQR ring, and a modified metal EQR ring 75. The starting wafer for the 600 volt device has an epitaxial layer 100 thickness of 61μm and resistivity of 21.5 ohm-cm. The novel 5 mask process for making the device of Figure 3 employs the steps used for the 400 volt device of Figure 2, except that a further mask step is used after step 8 above and following the B Br Ox step. Following this added mask step, there is a BOE etch for 17 minutes to open windows for the guard ring diffusions and the process continues as described for Figures 1 and 2.

[0016] In each of Figures 1, 2 and 3, the novel FRED device employs a single large P diffusion for the active area and platinum atoms for life time killing. In Figures 2 and 3, the device termination is covered with amorphous silicon.

[0017] Although the present invention has been described in relation to particular embodiments thereof, many other variations and modifications and other uses will become apparent to those skilled in the art.